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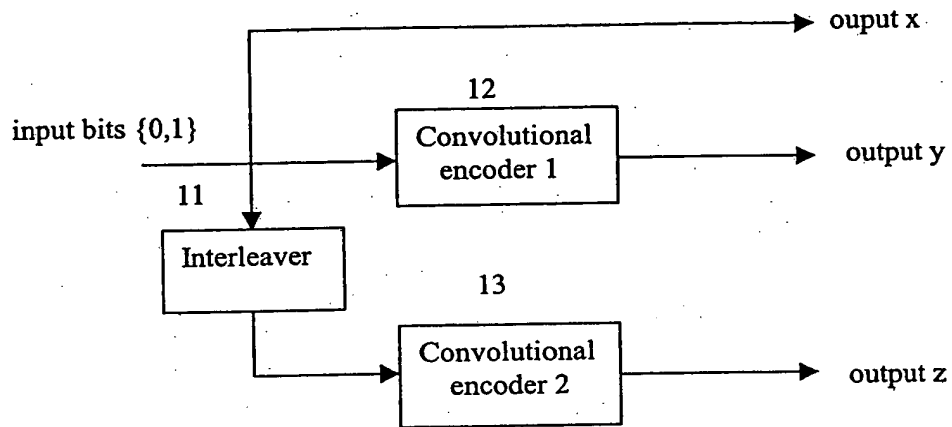


Figure 1 Basic Architecture of Turbo Encoder (Coding Rate = 1/3)

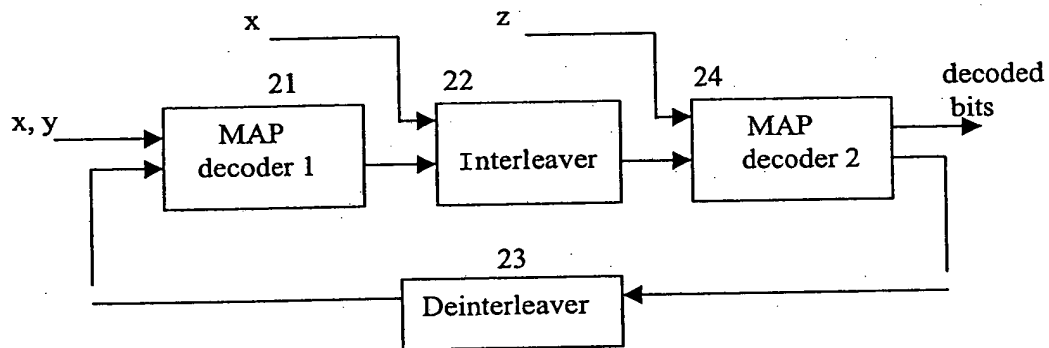


Figure 2 Basic Architecture of Turbo Decoder (Coding Rate = 1/3)

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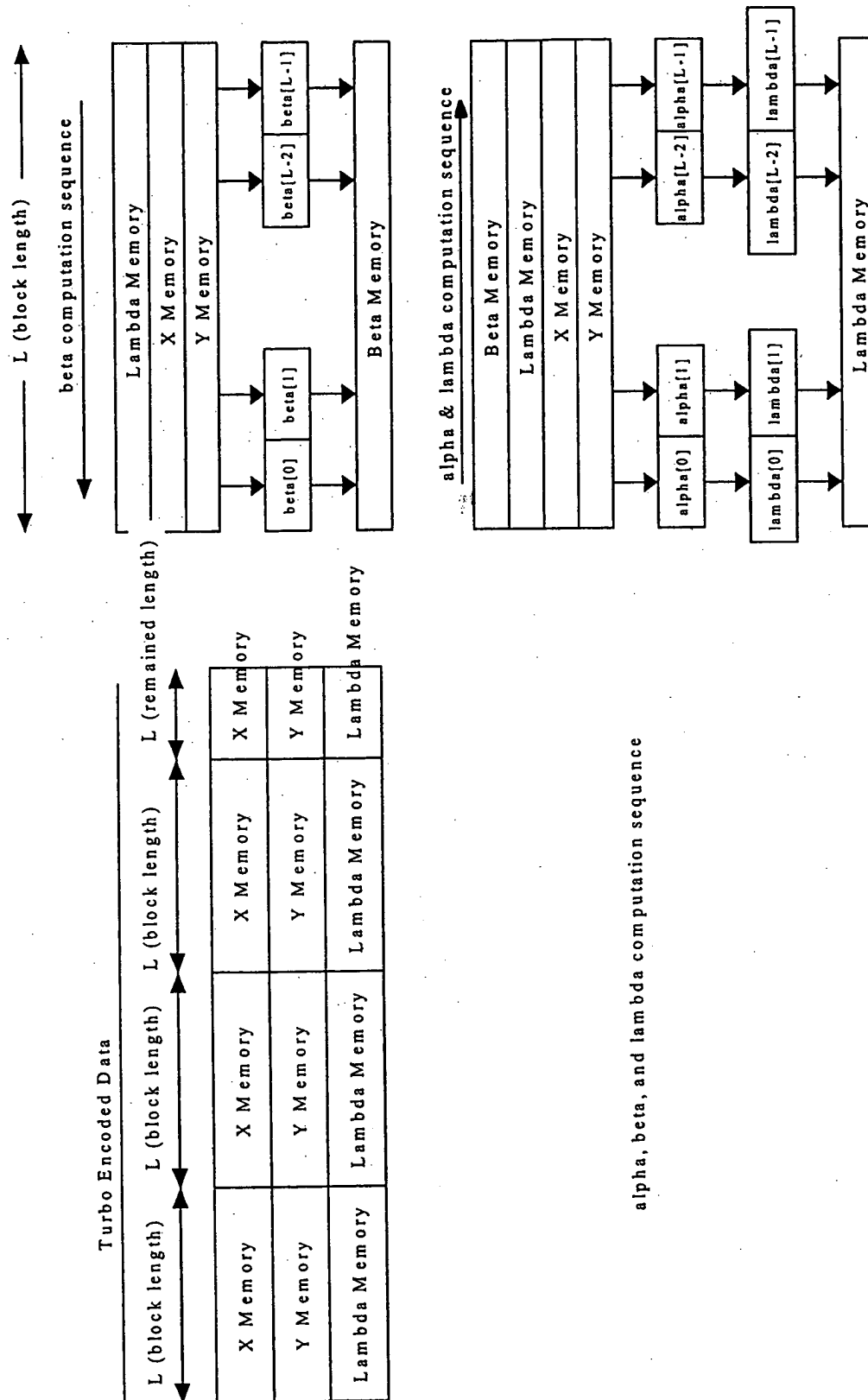


Figure 3. Alpha, Beta and Lambda Calculation Sequence

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State Transition in Beta Computation

State m	0	1	2	3	4	5	6	7
Next[m][0]	0	4	5	1	2	6	7	3
Next[m][1]	4	0	1	5	6	2	3	7

State Transition in Alpha Computation

State m	0	1	2	3	4	5	6	7
prev[m][0]	0	3	4	7	1	2	5	6
prev[m][1]	1	2	5	6	0	3	4	7

Figure 4 State Transition in Beta and Alpha Computation.

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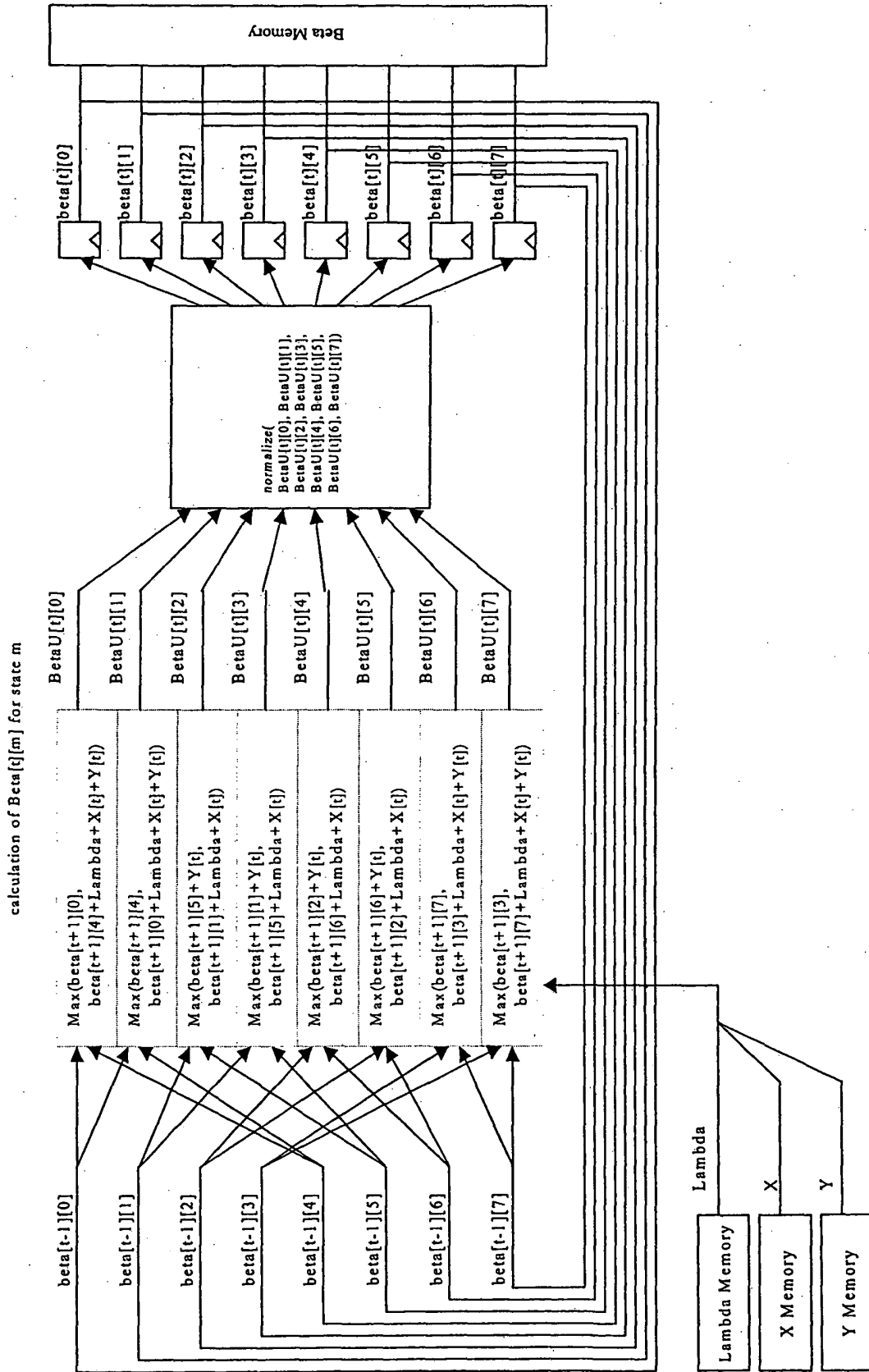


Figure 5. Beta Computation Block Diagram

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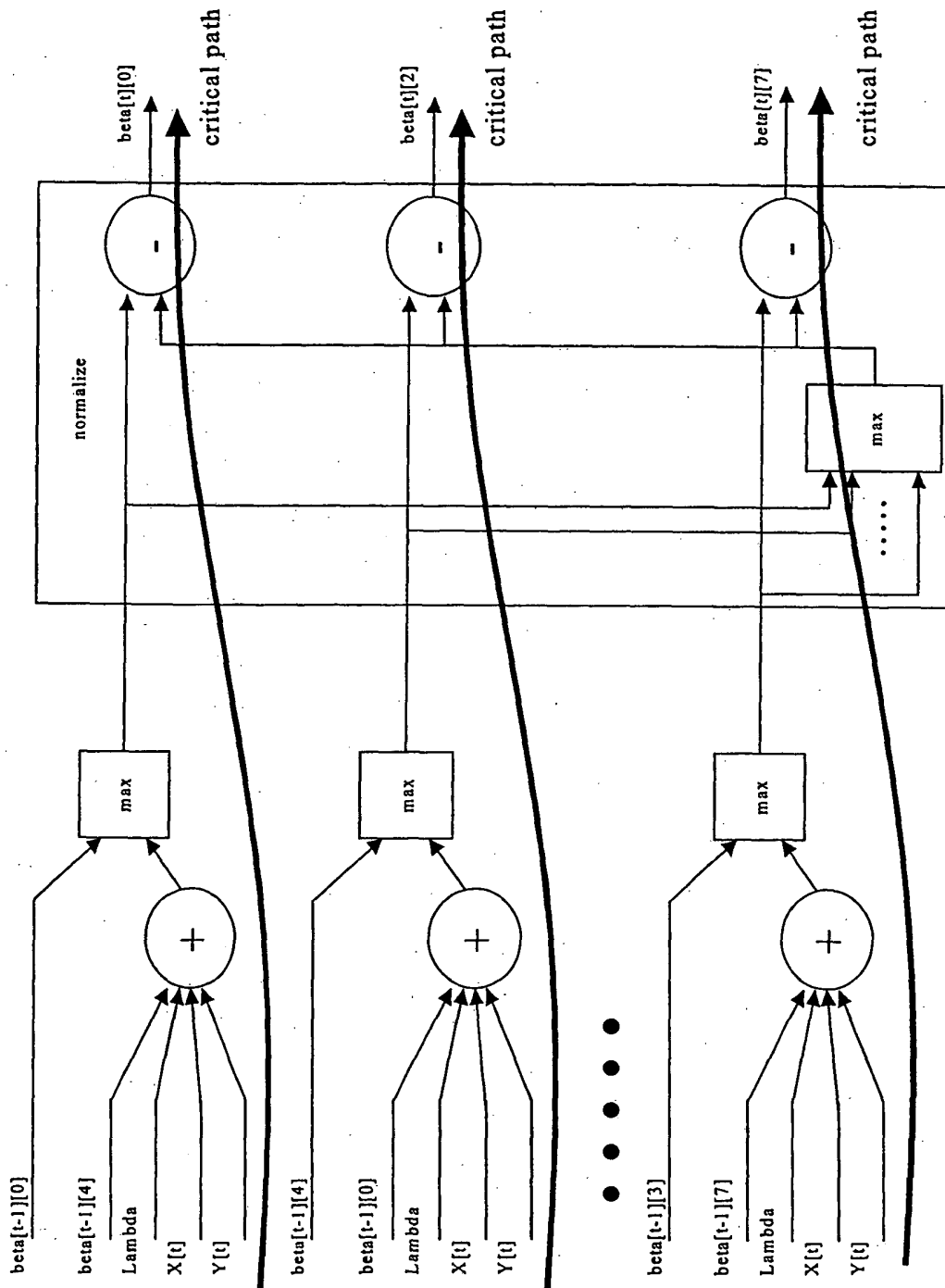


Figure 6 Details Beta Computation and Critical Path Block Diagram

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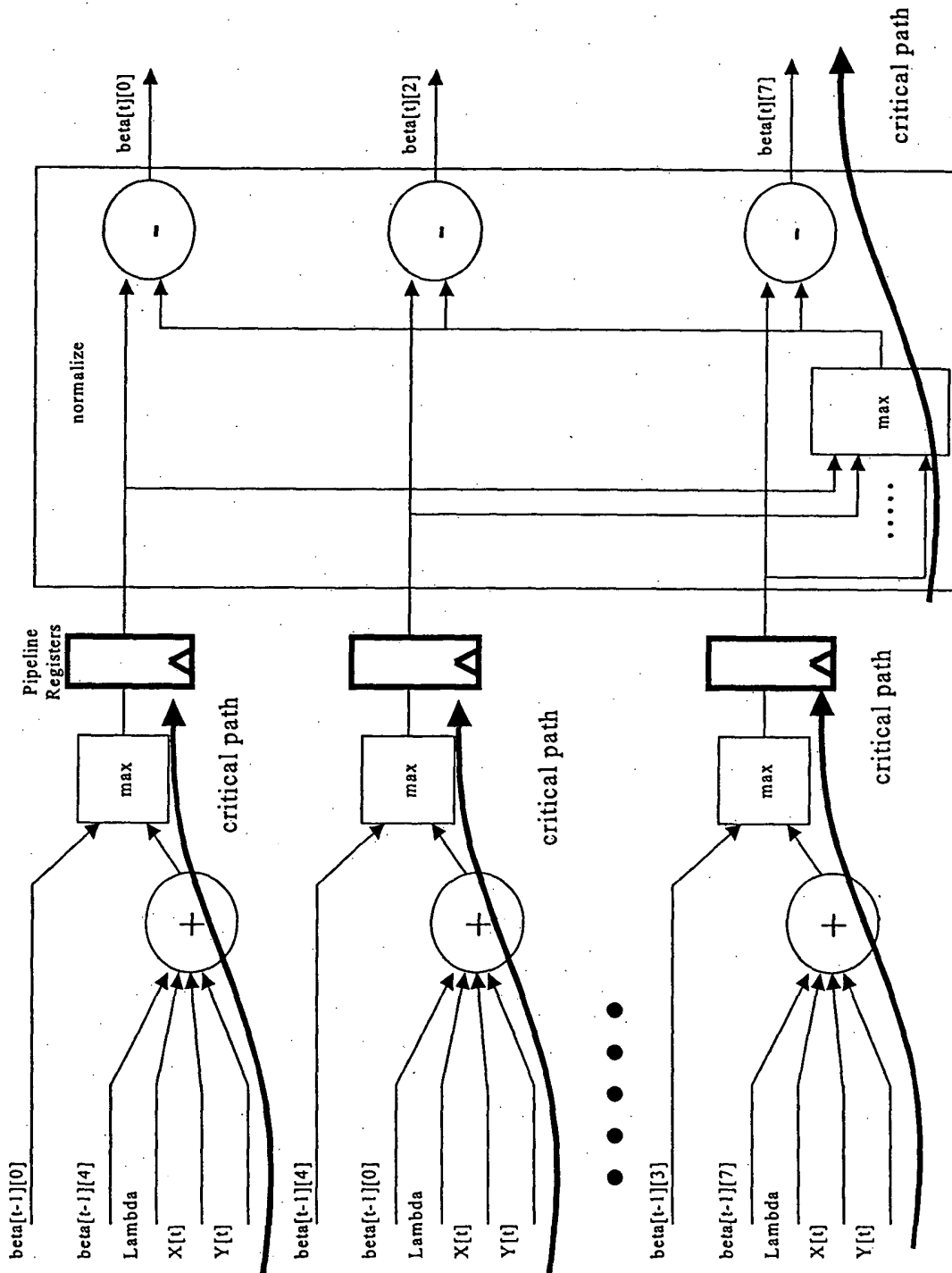


Figure 7: The Improved Structure of Beta Computation and Critical Path Diagram

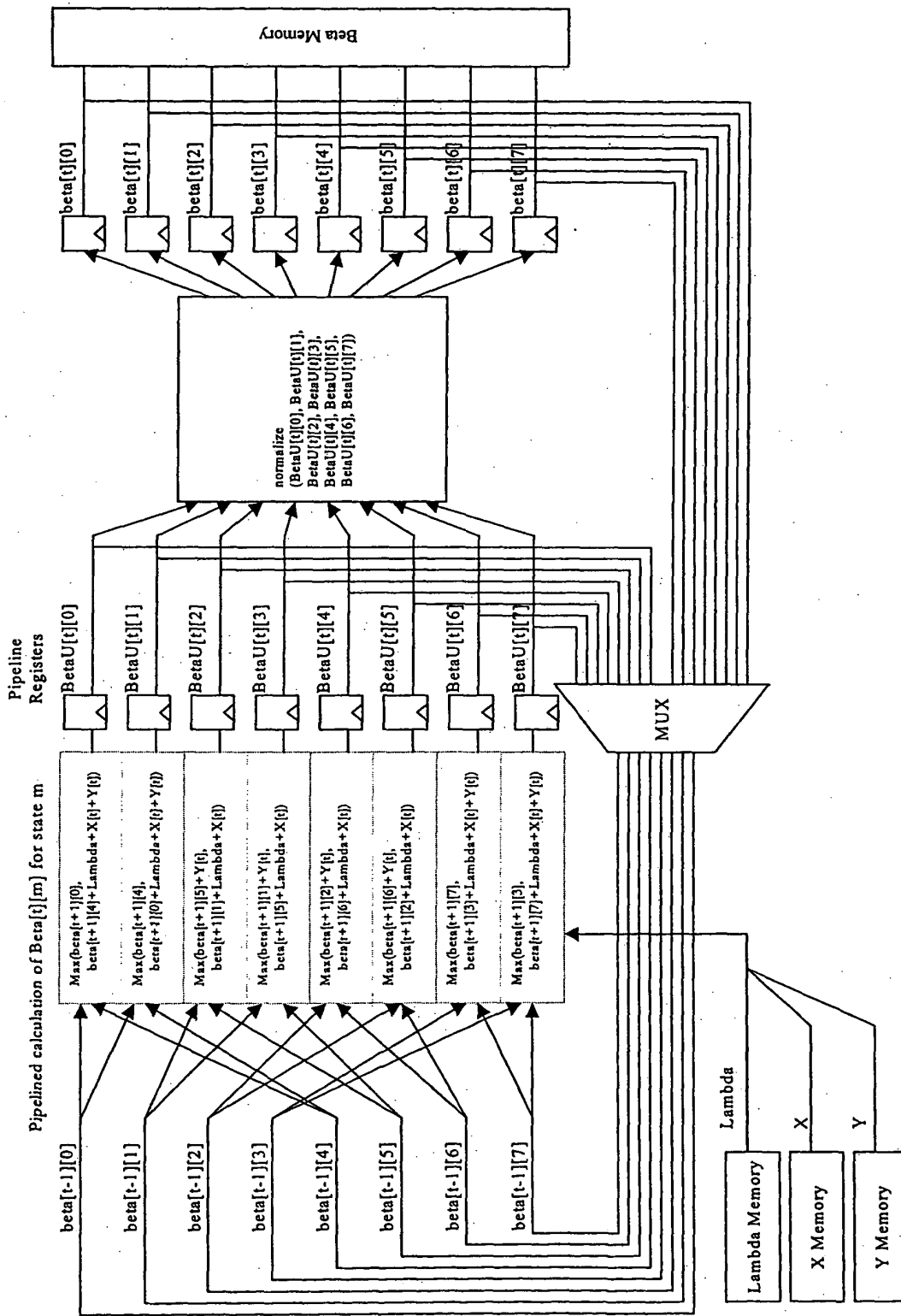


Figure 8 Overall Structure of Pipelined Beta Computation Path Diagram

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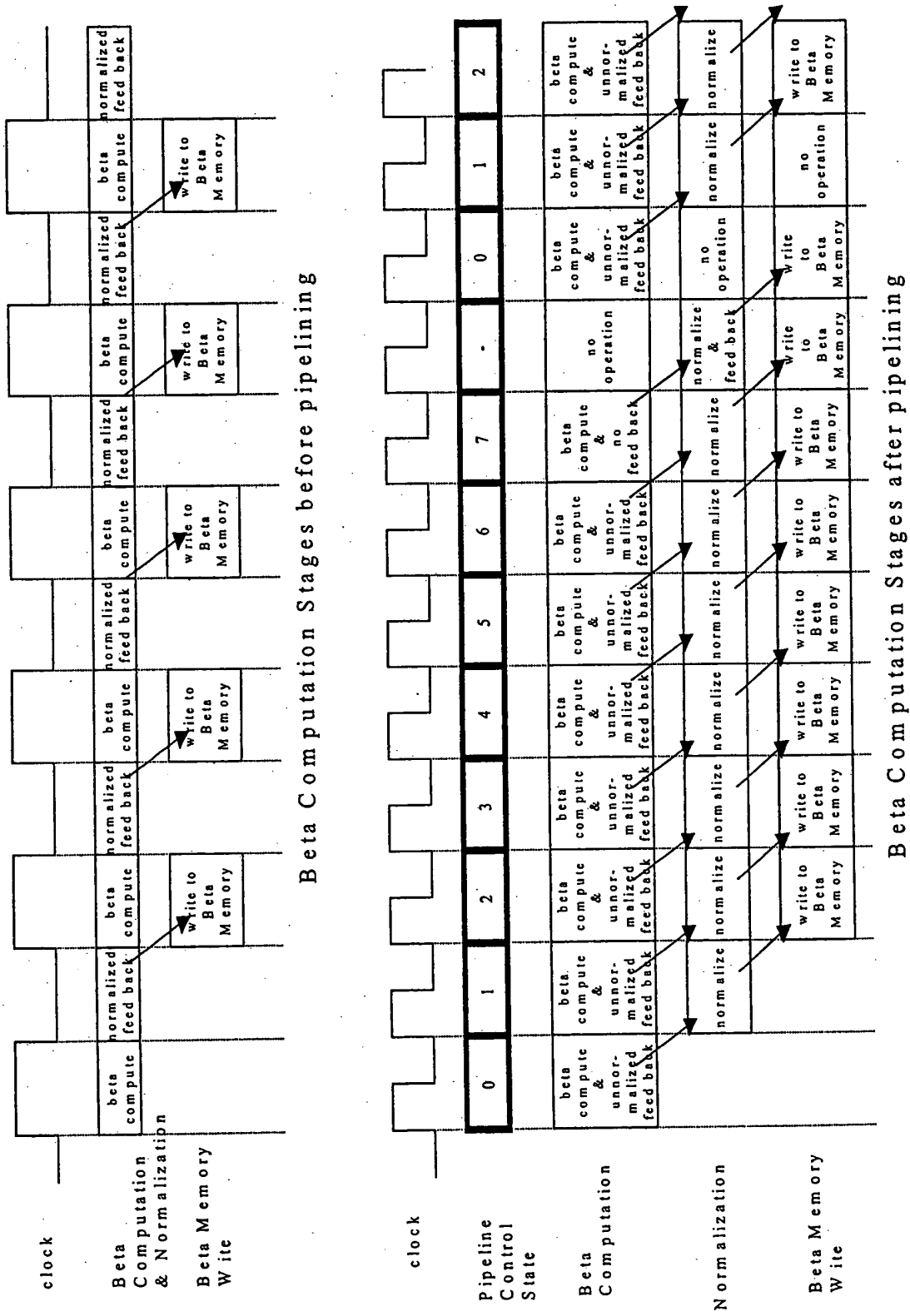


Figure 9 The pipeline Stages of Beta Computation Diagram

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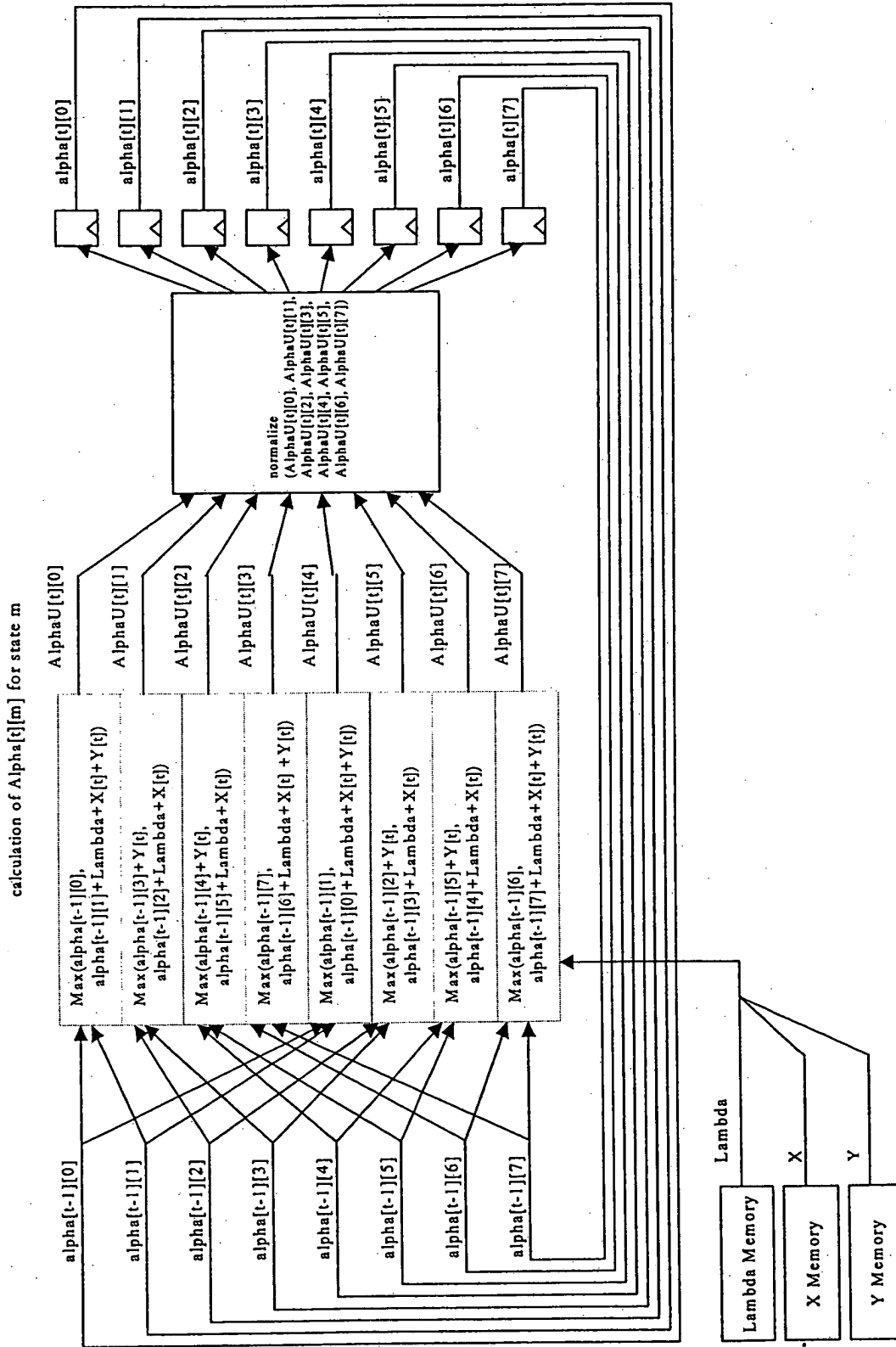
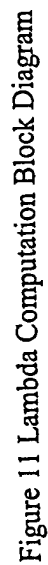


Figure 10 Alpha Computation Block Diagram



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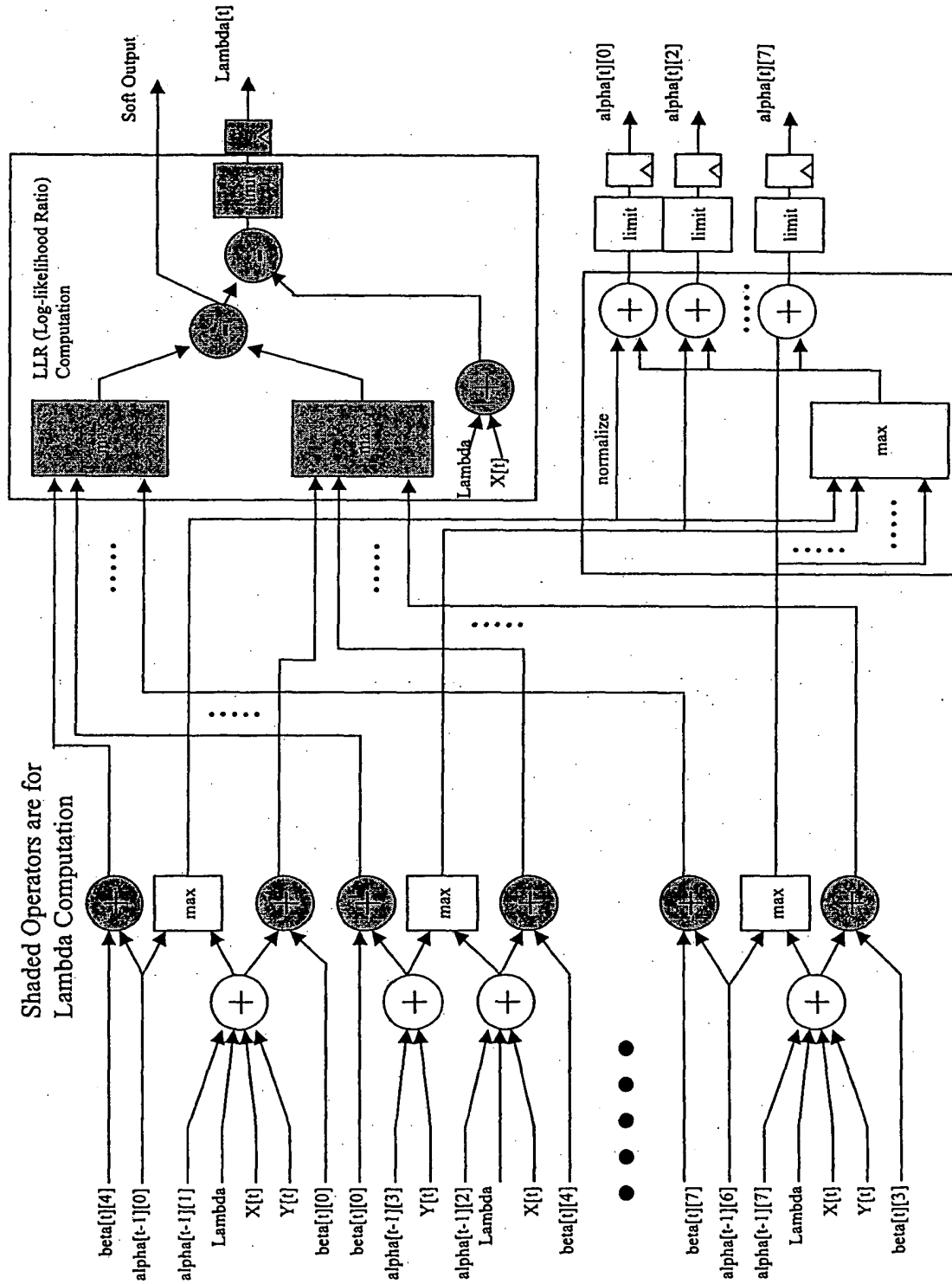


Figure 12 Details Alpha and Lambda Computation and Critical Path Block Diagram

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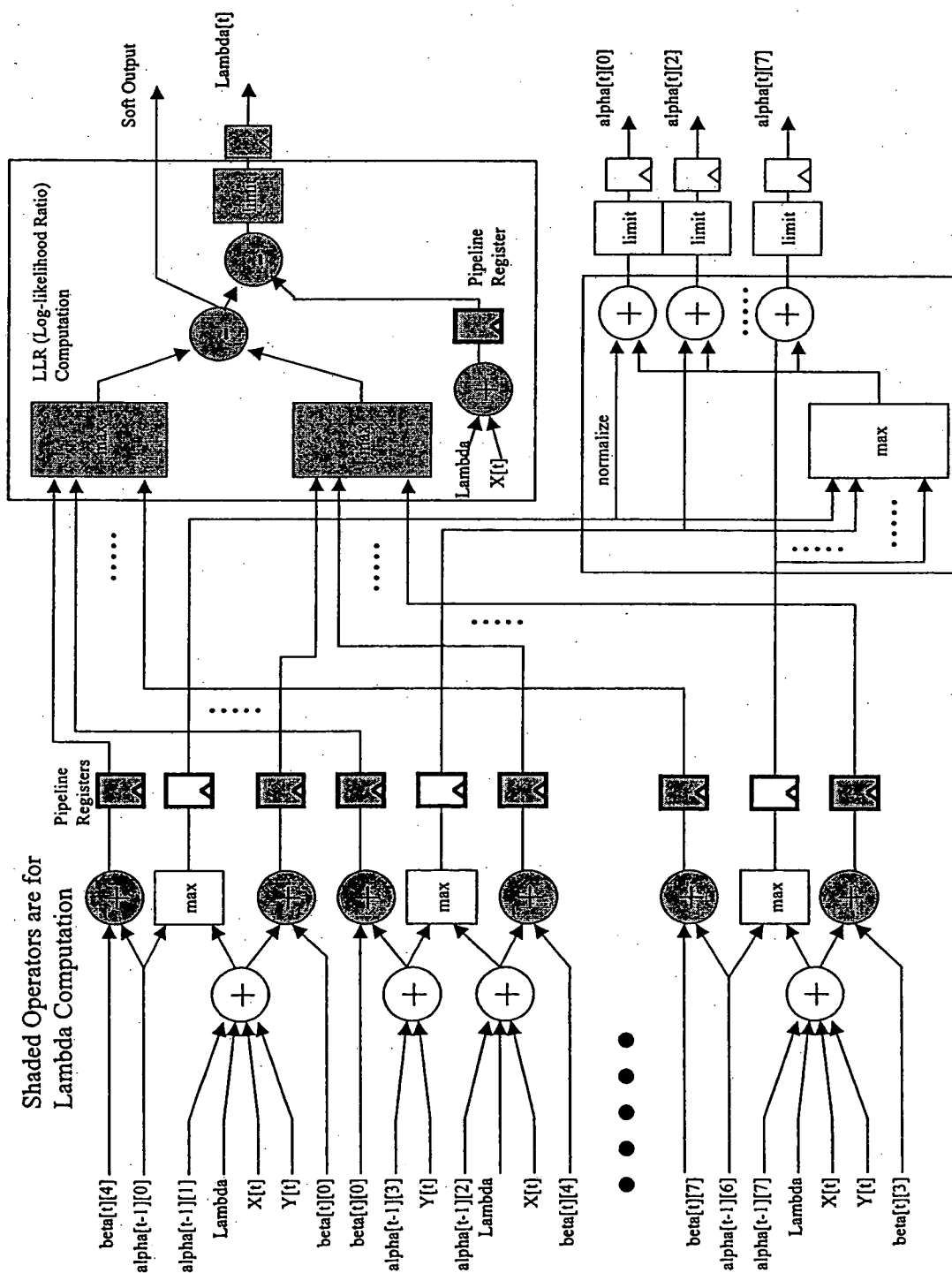


Figure 13 Improved Structure of Alpha and Lambda Computation and Critical Path Diagram

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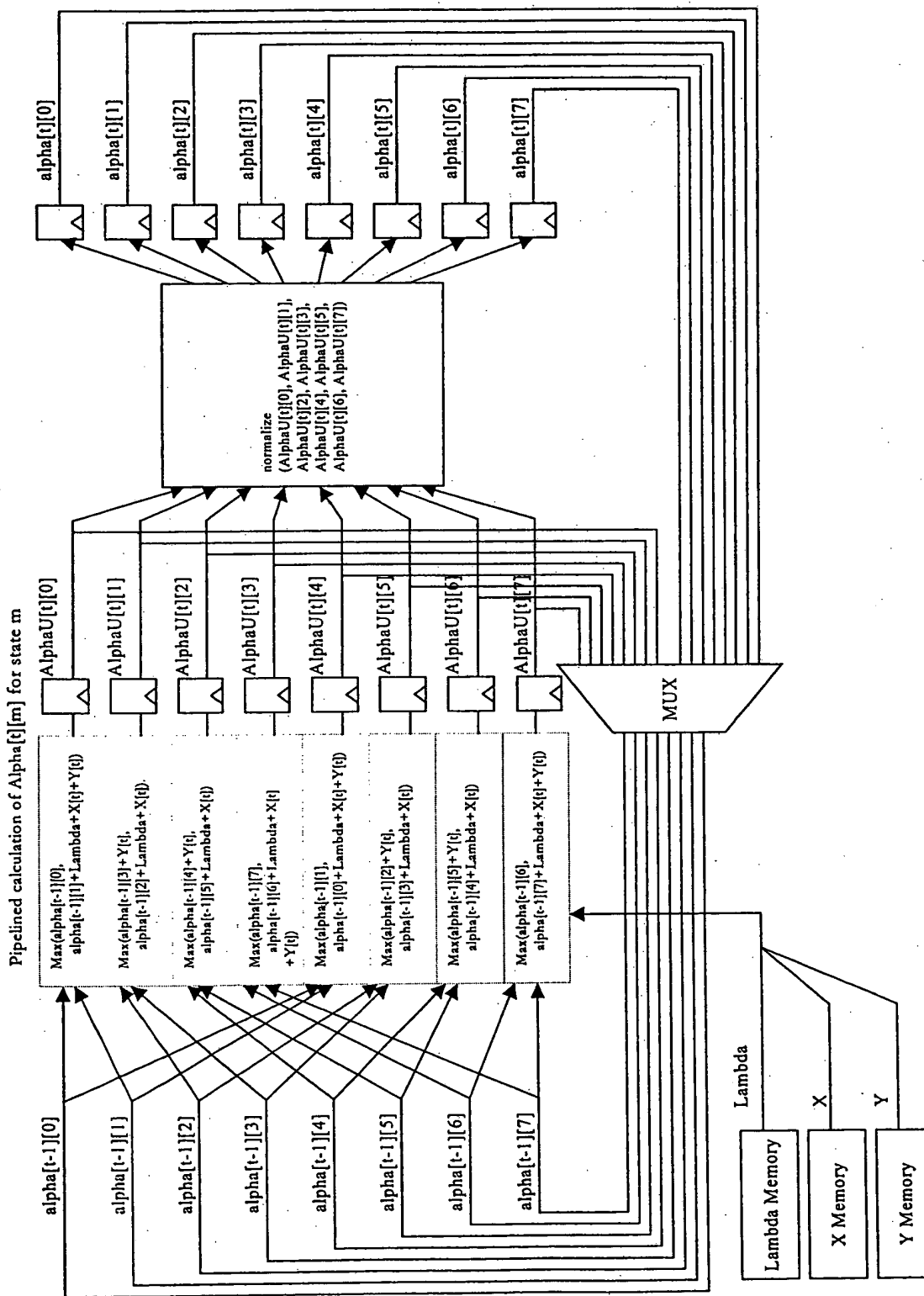


Figure 14 The Overall Structure of Pipelined Alpha Computation Path Diagram

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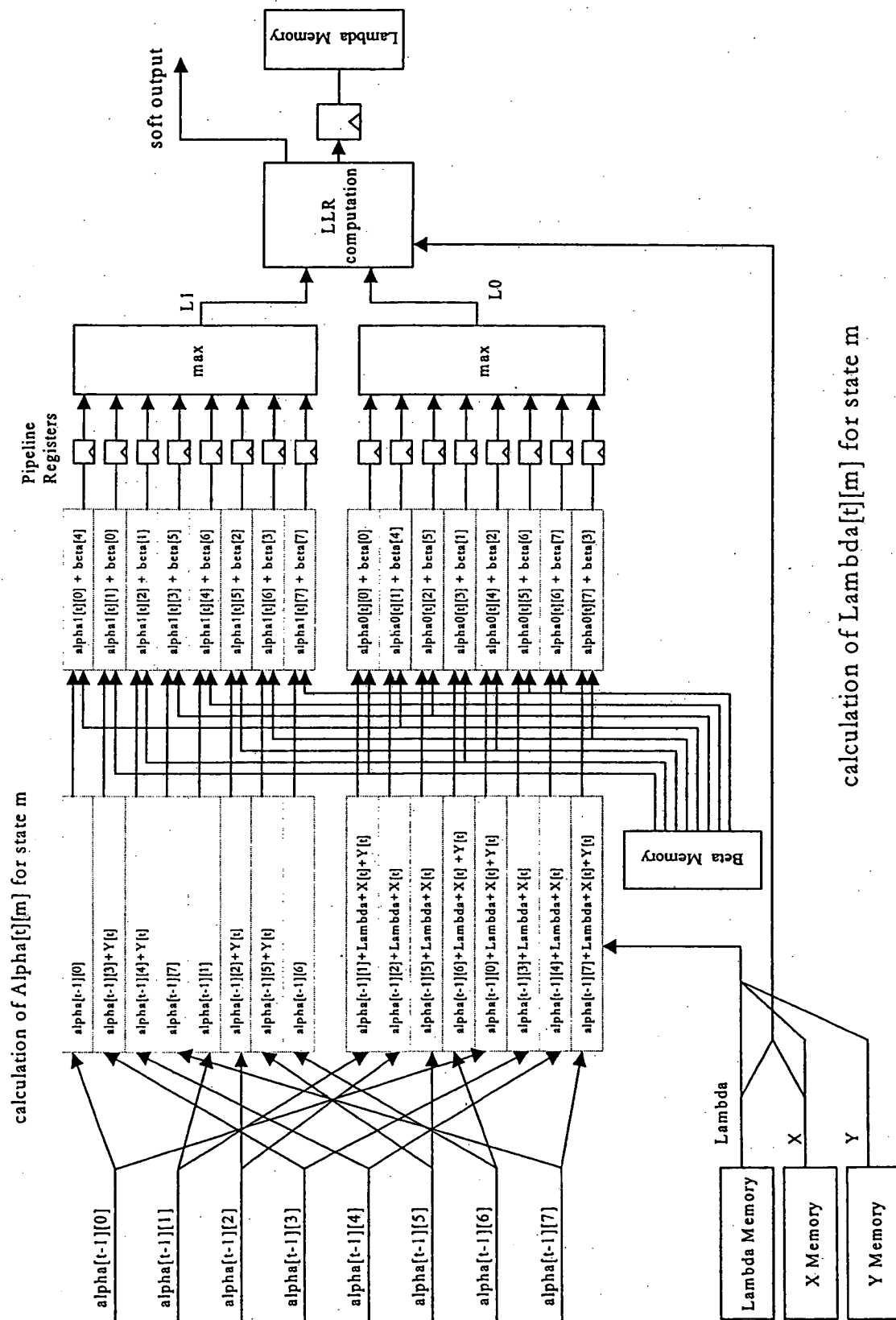


Figure 15 The Overall Structure of Pipelined Lambda Computation Path Diagram

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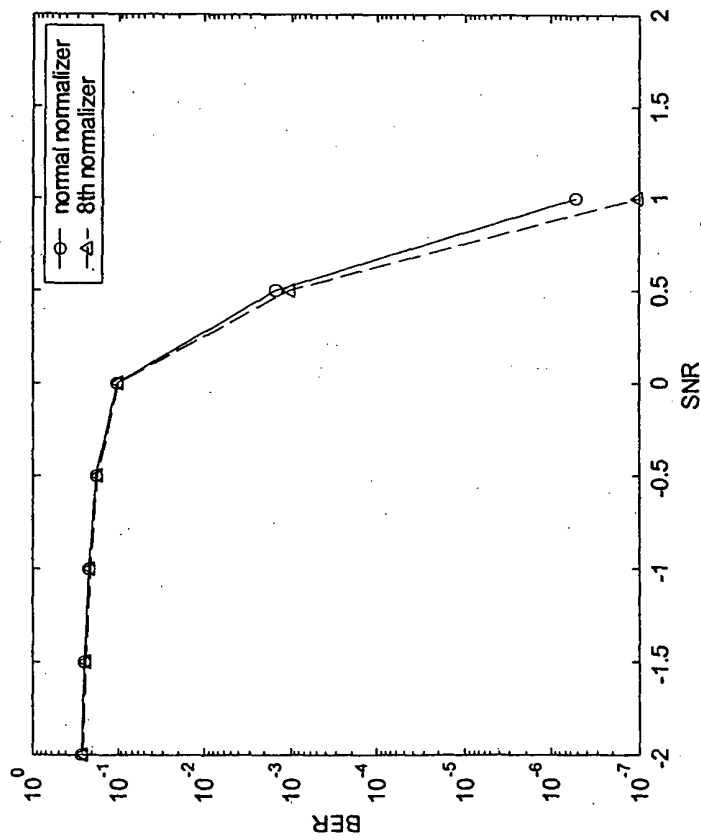


Figure 16 BER and SNR simulation for original normalization and new normalization
Block length = 3856 bits)

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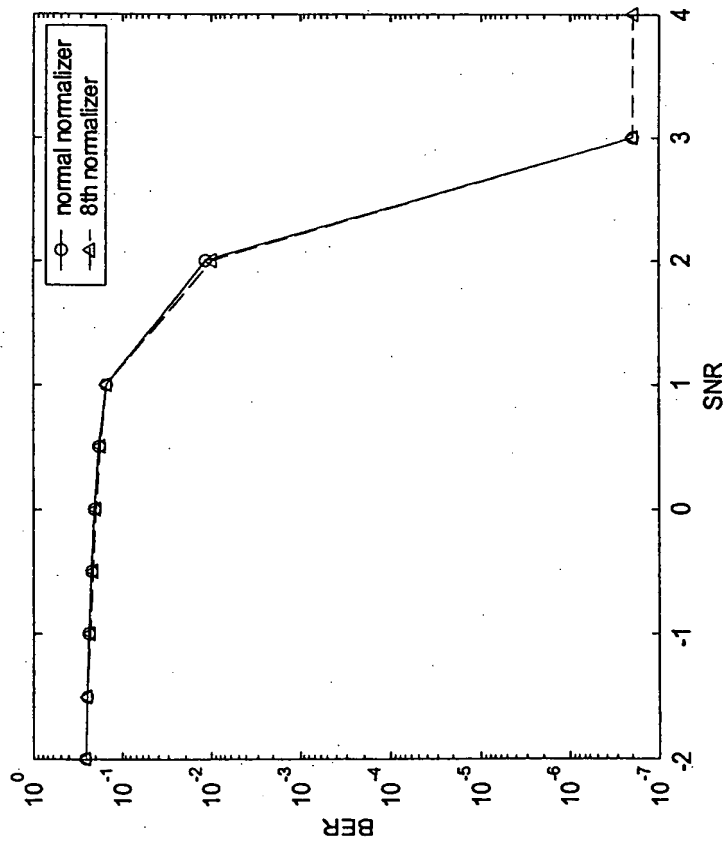


Figure 17 BER and SNR simulation for original normalization and new normalization
(Block length = 5114 bits)